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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,115	01/30/2004	Young Hoon Kwark	YOR920030625US1 (163-27)	7189

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,115	KWARK, YOUNG HOON	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recited "**to determine actions to remedy problems prior to completing fabrication of integrated circuits on the integrated circuit substrate"** in claims 1 and 10 and the recited "**partially fabricated**" in claim 10 are not mentioned in the specification.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recited **test device including the source** recited in claim 10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2,4,7-10,12,15-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore US Patent No. 6,759,863 in view of Min et al US Patent No. 6,556.029.

With respect to the claims 1 and 9, Moore ('863) expressly discloses a wireless IC test system (see Figs. 1-7) for measuring circuits (IC 18) on an integrated circuit substrate (wafer 16) during fabrication (see Col. 1, line 9, " during the IC fabrication process") as claimed, comprising:

a measurement circuit (test circuit 14) formed on the integrated circuit substrate (16) which measures at least one characteristic (see claim 2, "parametric test") of an integrated circuit (18),

The measurement circuit (14) comprising a power transfer device (see Fig. 7) including a power transfer component (50,52,54,56 68), which receives energy (RF power signal 32 from a source (12) where the source 12 does not make physical contact with the integrated circuit substrate (16) to transfer power to the measurement circuit (14) , the measuring circuit (14) including components (see Fig. 7 and Col. 8, lines 43-44, " to send the test result 34 from the test circuit 14 to the test unit 12) so that process parameters are measured for the components to provide information about processing steps and " to determine actions to remedy problems prior to completion fabrication of integrated circuits on the integrated circuit substrate (see Col. 19, lines 8-20).

Moore ('863) does not disclose that his measurement circuit (14) includes components that mirror behavior of the integrated circuit.

Min et al ('029) disclose an apparatus (see Figs. 2-3) for optical beam induced current investigation in integrated circuit comprising a measuring circuit (80) which includes components (82) that mirror behavior of the integrated circuit (see Col. 2, lines 45-46 " imaging of semiconductor junctions on an integrated circuit ").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the components for mirroring the integrated circuit as taught by Min et al ('029) into Moore ('863)'s measuring circuit for the expected advantage of testing the integrated circuit without the need for probing of interior portion of the circuit as disclosed by Min et al ('029) (see Col. 1, lines 65-66).

With respect to the claims 10 and 19, Moore ('863) discloses a wireless IC test system (see Figs. 1-7) for measuring circuits on an integrated circuit substrate as claimed, comprising:

A semiconductor wafer (16) including a plurality of chips (18);

a measurement circuit (test circuit 14) formed on at last one of the chips and configured to measures at least one characteristic (see claim 2, parametric test) of a "partially fabricated" integrated circuit (see Col. 1, line 9, " during the IC fabrication process),

The measurement circuit (14) comprising a power transfer device (see Fig. 7, 50, 52) which receives energy RF power signal 32 from a test unit including a source (12) where the source 12 does not make physical contact with the integrated circuit substrate (16) to transfer power to the measurement circuit (14) , the measuring circuit (14) including components (see Fig. 7 and Col. 8, lines 43-44, " to send the test result 34 from the test circuit 14 to the test unit 12) so that process parameters are measured for the components to provide information about processing steps and " to determine actions to remedy problems prior to completion fabrication of integrated circuits on the integrated circuit substrate (see Col. 19, lines 8-20).

Moore ('863) does not disclose that his measurement circuit (14) includes components that mirror behavior of the integrated circuit and the test device (12) operates in alignment with the power transfer component.

Min et al ('029) disclose an apparatus (see Figs. 2-3) for optical beam induced current investigation in integrated circuit comprising a measuring circuit (80) which

includes components (82) that mirror behavior of the integrated circuit (see Col. 2, lines 45-46 " imaging of semiconductor junctions on an integrated circuit ") and a test device including a source (38), which delivers energy to the power transfer component (42) when in alignment with the power transfer component (42) (see Col. 3, lines 9-12 " in alignment") .

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the components for mirroring the integrated circuit and the alignment feature as taught by Min et al ('029) into Moore ('863)'s measuring circuit for the expected advantage of testing the integrated circuit without the need for probing of interior portion of the circuit as disclosed by Min et al ('029) (see Col. 1, lines 65-66).

With respect to the claim 2, Moore ('863) discloses that the integrated circuit substrate includes a chip (18) formed on a semiconductor wafer (16) (see Fig. 2).

With respect to claims 4 and 12, Moore ('863) discloses that the source (12) transfers energy via inductive coupling (see Col. 7, lines 56-65).

With respect to claims 7 and 15, Moore ('863) discloses capacitive coupling (see claim 18).

With respect to claims 8 and 16, Moore ('863) discloses that his measuring circuit (14) includes a control circuit (see Fig. 7, 62,66,68) which conveys measuring information (see Col. 20, lines 41-42).

3. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore ('863) in view of Min et al ('029) as applied to claims 1 and 10 above, and further in view of Fischer et al US patent No. 6,787,801.

Moore ('863) in view of Min et al ('029) do not disclose that the measurement circuit (2) is formed in a kerf area of the chip (1).

Fischer et al ('801) disclose a system for measuring circuits on an integrated circuit substrate comprising a measurement circuit (3) and exclusively teach that the measurement circuit (3) is formed in a kerf area (4) of the chip (1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the feature of having measurement circuit formed in the kerf area of the chip as taught by Fischer et al ('801) into Moore ('863) in view of Min et al ('029)'s system for the expected benefit of providing an improved wafer design for testing integrated circuits on the wafer as disclosed by Fischer et al ('801) (see C0l. 2, lines 45-46).

4. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore ('863) in view of Min et al ('029) as applied to claims 1 and 10 above, and further in view of Hirt US Patent No. 6,686,760.

Moore ('863) in view of Min et al ('029) do not disclose that the power transfer device (6) includes a photo sensor and the source (30) transfers energy via light.

Hirt ('760) discloses a photosensor for testing an integrated circuit (see Fig. 2) and exclusively teach that a power transfer device includes photo sensor (see Fig. 2) and the source (see Fig. 9, 306) transfers energy via light (see Col. 5, lines 46-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of transferring energy via light as taught by Hirt ('760) into Moore ('863) in view of Min et al ('029)'s system for the expected benefit of providing a system for contactless testing which allows for fast and reliable testing as disclosed by Hirt ('760) (see Col. 2, lines 4-5).

5. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore ('863) in view of Min et al ('029) and Hirt ('760) as applied to claims 1, 5, 10 and 13 above, and further in view of Cook et al US Publication No. 2002/0047722.

Moore ('863) in view of Min et al ('029) and Hirt ('760) do not disclose that the photo sensor includes a photodiode and that the source includes a laser.

Cook et al ('722) disclose a contact-less probe of semiconductor wafers (see Figs 1 and 5) and exclusively teach a power transfer component includes photodiode (10) and a source (14) includes a laser (see page 3, paragraph (0046), line 6 " optical power source, such as a laser").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of photodiedo and laser as taught by Cook et al ('722) into Moore ('863) in view of Min et al ('029) and Hirt ('760) 's system for the expected benefit of providing a testing devices which do not contact the device under test (DUT) as disclosed by Cook et al ('722) (see page 1, paragraph (0002)).

6. Claims 17-18 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore ('863) in view of Min et al ('029) as applied to claim10 above, and further in view of Mullen US Patent No. 5,583,445.

Moore ('863) in view of Min et al ('029) do not disclose that the test device includes a thin film dielectric membrane having the source mounted thereon and includes a probe ring .

Mullen ('445) discloses an opto-electronic membrane probe (see Fig. 6) which includes a thin film dielectric membrane (62) having the source (64, 68) mounted thereon (see Col. 8, lines 17-18) and includes a probe ring (a support for the thin film dielectric membrane (62)). Furthermore, Mullen ('445) discloses that his thin film dielectric membrane (62) is transparent so that the source (64,68) mounted thereon can be visually aligned to the power transfer component (see Col. 5, lines 44-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the thin film dielectric membrane (62) of Mullen ('445) into Moore ('863) in view of Min et al ('029) and Hirt ('760) 's system for the expected benefit of providing a opto-electronic membrane probe which relates to testing a high speed circuit with minimized mechanical damage to the circuit 's pads as disclosed by Mullen ('445) (see Col. 1, lines 6-10).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Conn US Patent No. 6,815,973 discloses a testing system comprising on chip test circuit and power transfer device (see Figs. 1-14).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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